Customer No.: 31561
Application No.: 10/711,939
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AMENDMENT

To the Claims:

1. (original) A dynamic random access memory (DRAM) cell, comprising:

a semiconductor pillar on a substrate;

a capacitor on a lower portion of a sidewall of the pillar, comprising:

a first plate in the lower portion of the sidewall of the pillar;

a second plate as an upper electrode at periphery of the first plate;

a third plate at periphery of the second plate, electrically connecting with the first plate to form a lower electrode together; and

a dielectric layer, separating the second plate from the first plate and the third plate; and

a vertical transistor on an upper portion of the sidewall of the pillar, electrically coupled with the capacitor.

2. (original)The DRAM cell of claim 1, wherein

the first plate and the third plate are electrically connected via a design wherein the first plate further extends to the substrate beside the pillar and the third plate contacts with the substrate beside the pillar; and

the dielectric layer is also disposed on a portion of the first plate in the substrate beside the pillar to separate a bottom of the second plate from the first plate.

3. (original) The DRAM cell of claim 2, wherein the dielectric layer comprises:

a first dielectric layer between the pillar and the second plate and between the substrate and the second plate; and

a second dielectric layer between the second plate and the third plate, connecting with the first dielectric layer.

4. (original) The DRAM cell of claim 1, wherein the second plate has a top portion directly contacting with a source/drain region of the vertical transistor in the pillar.

5. (original) The DRAM cell of claim 1, wherein the first plate, the second plate, the third plate and the dielectric layer surround the pillar.

6. (original)The DRAM cell of claim 5, wherein the capacitor further comprises:

a collar insulating layer surrounding the pillar and covered by an upper portion of the second plate.

7. (original)The DRAM cell of claim 6, wherein the second plate comprises:

a first conductor surrounding the collar insulating layer;

a second conductor under the first conductor and the collar insulating layer; and

a third conductor on the first conductor and the collar insulating layer, electrically coupled with the vertical transistor.

8. (original) The DRAM cell of claim 1, wherein the vertical transistor comprises,

a first doped region in the sidewall of the pillar, electrically connected with the upper electrode of the capacitor;

a second doped region in a top portion of the pillar;

a gate on the sidewall of the pillar between the first doped region and the second doped region; and

a gate insulating layer between the sidewall of the pillar and the gate.

9. (original) The DRAM cell of claim 8, wherein the gate is separated from a top portion of the upper electrode by an insulator.

10. (original) The DRAM cell of claim 8, wherein the first doped region, the gate and the gate insulating layer surround the pillar.

11. (original) A dynamic random access memory (DRAM) array, comprising:

rows and columns of memory cells disposed on a substrate, each comprising:

a semiconductor pillar on the substrate;

a capacitor on a lower portion of a sidewall of the pillar, comprising a first plate in the lower portion of the sidewall of the pillar, a second plate as an upper electrode at periphery of the first plate, a third plate disposed at periphery of the second plate and electrically connected with the first plate to form a lower electrode together, and a dielectric layer separating the second plate from the first plate and the third plate; and

a vertical transistor on an upper portion of the sidewall of the pillar, electrically coupled with the capacitor;

a plurality of bit lines, each coupled with one row of vertical transistors; and

a plurality of word lines, each coupled with one column of vertical transistors.

12. (original) The DRAM array of claim 11, wherein

the first plates are electrically connected with each other via a doped surface layer of the substrate between the pillars;

the third plates together constitute a conductive layer partially filling the space between the pillars and contacting with the doped surface layer of the substrate; and

the first plates, the doped surface layer and the conductive layer together serve as

a common lower electrode.

13. (original) The DRAM array of claim 12, wherein in each memory cell, the dielectric layer comprises:

a first dielectric layer between the second plate and the pillar and between the second plate and the doped surface layer of the substrate; and

a second dielectric layer between the second plate and the third plate, connecting with the first dielectric layer.

14. (original) The DRAM array of claim 11, wherein each second plate has a top portion directly contacting with a source/drain region of a corresponding vertical transistor.

15. (original) The DRAM array of claim 11, wherein in each capacitor, the first plate, the second plate, the dielectric layer and the third plate surround the pillar.

16. (original) The DRAM array of claim 15, wherein each capacitor further comprises a collar insulating layer that surrounds the corresponding pillar and is covered by an upper portion of the second plate.

17. (original) The DRAM array of claim 16, wherein the second plate comprises:

a first conductor surrounding the collar insulating layer;

a second conductor under the first conductor and the collar insulating layer; and

a third conductor on the first conductor and the collar insulating layer, electrically coupled with a corresponding vertical transistor.

18. (original) The DRAM array of claim 11, wherein each vertical transistor comprises:

a first doped region in the sidewall of a corresponding pillar, electrically connected with the upper electrode of a corresponding capacitor;

a second doped region in a top portion of the pillar;

a gate on the sidewall of the pillar between the first doped region and the second doped region; and

a gate insulating layer between the sidewall of the pillar and the gate.

19. (original) The DRAM array of claim 18, wherein each bit line directly contacts with the second doped regions of the vertical transistors of the memory cells in one row.

20. (original) The DRAM array of claim 18, wherein the gates of the memory cells in one column are connected to each other to form a gate line.

21. (original) The DRAM array of claim 20, wherein the gate line directly serves as a word line for the vertical transistors in the column.

22. (original) The DRAM array of claim 20, wherein a word line is electrically connected to the gate line via at least one contact between two pillars.

23-40 (cancelled).